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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/664,910 | 09/18/2000 | John Halbert | 81674-027 1623 | 4433 |

7590 12/30/2003

Pillsbury Winthrop LLP
Intellectual Property Group
725 South Figueroa Street
Suite 2800
Los Angeles,, CA 90017-5406

| EXAMINER | |
|---|---|
| GANDHI, DIPAKKUMAR B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | |

DATE MAILED: 12/30/2003

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 452 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 452 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.



PTOL-85 (Rev. 11/03) Approved for use through 04/30/2004.

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# NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 12/30/2003

Pillsbury Winthrop LLP
Intellectual Property Group
725 South Figueroa Street
Suite 2800
Los Angeles,, CA 90017-5406

| EXAMINER | |
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TITLE OF INVENTION: MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1330 | $0 | $1330 | 03/30/2004 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

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If the SMALL ENTITY is shown as NO:

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B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**



PTOL-85 (Rev. 11/03) Approved for use through 04/30/2004.

## PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail** **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

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Pillsbury Winthrop LLP
Intellectual Property Group
725 South Figueroa Street
Suite 2800
Los Angeles,, CA 90017-5406

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/664,910 | 09/18/2000 | John Halbert | 81674-027 1623 | 4433 |

TITLE OF INVENTION: MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1330 | $0 | $1330 | 03/30/2004 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| GANDHI, DIPAKKUMAR B | 2133 | 714-718000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ❑ individual ❑ corporation or other private group entity ❑ government

4a. The following fee(s) are enclosed:

❑ Issue Fee
❑ Publication Fee
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):

❑ A check in the amount of the fee(s) is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date)

NOTE; The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/664,910 | HALBERT ET AL. | |
| | Examiner | Art Unit | |
| | Dipakkumar Gandhi | 2133 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Pre-Amendment B dated 10/14/2003*.
2. ☒ The allowed claim(s) is/are *1-64*.
3. ☒ The drawings filed on *18 September 2000* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the margin according to 37 CFR 1.121(d).**

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No. _____
4☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5☐ Notice of Informal Patent Application (PTO-152)
6☐ Interview Summary (PTO-413), Paper No._____ .
7☐ Examiner's Amendment/Comment
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other .

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

***Allowable Subject Matter***

1. Claims 1-64 are allowed.

2. Preliminary Amendment B dated 10/14/2003 has been entered.

3. The following is an examiner's statement of reasons for allowance:

- **Amended independent claim 1** recites a memory component with built-in self test, comprising: an input/output interface having a loopback; a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and a compare register to store and compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer

The prior art of record does not teach or fairly suggest these limitations. The Gillingham reference teaches a semiconductor device having a self test circuit including an embedded dynamic random access memory for storing data, a self test controller for internally generating test data patterns and expected resulting data and for comparing the expected resulting data with actual resulting data and test interface circuitry for loading the test data patterns into the memory and reading back the actual resulting data from the memory (abstract, Gillingham). However the Gillingham reference shows that the BIST controller is external of the memory component that contains the memory array (DRAM) and not within a memory component residing in a memory module.

The Bates reference teach that I/O loopback tests are carried out by providing data from a functional logic block (or FLB) within the IC and driving the data out through the output component of each I/O buffer (col. 1, lines 33-37, Bates et al.). However Bates reference also teaches that a method and apparatus for performing an I/O loopback test without using core logic within a FLB is desired (col. 1, lines 48-50, Bates et al.). The Bates reference teaches that it is not desirable to perform I/O loopback tests wherein a system processor performs the testing as is typically done. Therefore, the Bates reference does not teach the use of a controller. The Bates reference also makes no mention of a compare register within the compare unit 220 for storing input/output test data. Thus the Bates reference makes no mention of a

controller or a compare register within a memory component. Therefore, the Gillingham and Bates references do not teach the memory component of independent claim 1.

Hence claim 1 is allowed.

- Claims 2-8 are allowed because of the combination of additional limitations and the limitations listed above.
- **Amended independent claim 16** recites limitations similar to independent claim 1, as amended. Hence claim 16 is allowed.
- Claims 17-23, 60-61 and 62-64 are allowed because of the combination of additional limitations and the limitations listed above.
- **Amended independent claim 9** recites a memory component with built-in self test, comprising: a memory array; an input/output interface coupled to the memory array and having a loopback; a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and a compare register to store and compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

The prior art of record does not teach or fairly suggest these limitations. The Gillingham reference teaches a semiconductor device having a self test circuit including an embedded dynamic random access memory for storing data, a self test controller for internally generating test data patterns and expected resulting data and for comparing the expected resulting data with actual resulting data and test interface circuitry for loading the test data patterns into the memory and reading back the actual resulting data from the memory (abstract, Gillingham). However the Gillingham reference shows that the BIST controller is external of the memory component that contains the memory array, DRAM (figure 2, Gillingham) and not within a memory component residing in a memory module. The Gillingham reference also does not mention a compare register in the BIST controller. Therefore, the Gillingham reference does not teach the memory component of independent claim 9.

Hence claim 9 is allowed.

- Claims 10-15 are allowed because of the combination of additional limitations and the limitations listed above.
- **Amended independent claim 24** recites limitations similar to independent claim 9, as amended. The Gillingham reference does not teach storing the memory array test data transmitted to the memory array and the memory array test data read from the memory array in a register. Hence claim 24 is allowed.
- Claims 25-30 are allowed because of the combination of additional limitations and the limitations listed above.
- **Independent claim 31** recites a memory module with built-in self test, comprising: a plurality of memory components; an address and command buffer adapted to transmit address and command data and test data to one of the plurality of memory components, wherein the address and command buffer includes a register to receive a test result; and at least one data buffer to receive the test data from the address and command buffer, to receive the test data from one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from one of the plurality of memory components to generate the test result, wherein the plurality to memory components, the address and command buffer, and the at least one data buffer all reside within the memory module.

The prior art of record does not teach or fairly suggest these limitations. The Huang reference teaches a built in self test (BIST) for an embedded memory (abstract, Huang et al.). Huang et al. teach that data from the data composer 20 is also connected to the comparator 21 which received data out Q from the DRAM 13. The comparator compares the input data D from the data composer 20 to the output data Q from the DRAM 13 and outputs a go/no go signal BGO (figure 1, col. 4, lines 30-34, Huang et al.). The comparator 21 is in the sequencer circuit 12 and not in the DRAM interface buffer 14. Neither the data composer 20 or sequence controller 15 are contained within a buffer. Therefore, the Huang reference does not teach the memory module of independent claim 31.

The Osawa reference teaches that under the control of the self-test circuit 702, the register circuit 706 receives the test result upon the RAM test by the self-test circuit 702 (figure 142, col. 77, lines 62-64,

Osawa et al.). The register 706 is not in an address and command buffer as required by independent claim 31. Therefore, the Osawa reference does not teach the memory module of independent claim 31. Hence claim 31 is allowed.

- Claims 32-38 are allowed because of the combination of additional limitations and the limitations listed above.
- **Independent claims 39 and 48** recite limitations similar to independent claim 31. Hence independent claims 39 and 48 are allowed.
- Claims 40-47 are allowed because of the combination of additional limitations and the limitations listed above.
- Claims 49-53 are allowed because of the combination of additional limitations and the limitations listed above.
- **New independent claims 54 and 59** distinguish over the Gillingham and Bates references for the reasons mentioned above with respect to independent claim 1 and independent claim 16. The Gillingham and Bates references do not show a memory component with built-in self test having an input/output interface, a controller, and a compare register. The Gillingham and Bates references also do not show a controller to receive the memory array test data from the loopback of the input/output interface that was transmitted by the memory array to the input/output interface, and a compare register to store and compare the memory array test data transmitted to the memory array with the memory array test data received from the loopback of the input/output interface that was transmitted from the memory array, wherein the compare register generates a test result based on the memory array test data transmitted to the memory array compared with the memory array test data received from the loopback of the input/output interface that was transmitted by the memory array to the input/output interface. Hence independent claims 54 and 59 are allowed.
- Claims 55-58 are allowed because of the combination of additional limitations and the limitations listed above.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Dipakkumar Gandhi

Patent Examiner

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100